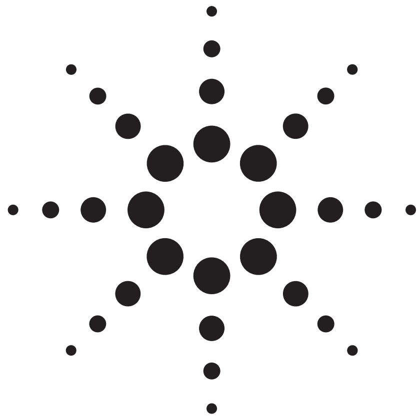

Agilent 4070 Series Accurate Capacitance Characterization at the Wafer Level

Application Note 4070-2

Agilent 4070 Series Semiconductor Parametric Tester

Agilent Technologies

Innovating the HP Way

Introduction

The continuing trend of decreasing device geometries of the next generation of ULSI devices is making precise characterization evaluation of semiconductor devices more and more critical.

Measurement of capacitance is used to determine oxide thickness, one of the key parameters of semiconductor devices. This oxide thickness is becoming thinner and thinner from generation to generation. Therefore, accurate capacitance measurement is very important in semiconductor process integration and process monitoring.

The Agilent 4070 series of semiconductor parametric testers perform accurate capacitance measurements, reliably and quickly.

In order for 4070 series testers to perform such precise measurements, appropriate fixturing and measurement techniques are required.

This application note describes the procedures required to precisely evaluate the capacitance of a Device Under Test (DUT) when using a 4070 series tester with an automatic wafer prober.

Factors Affecting the Measurement of Capacitance and Problem-Solving Techniques

Stray Capacitance and Residual Inductance

Cable and electrical leads in the measurement system behave like distributed electrical lines when a high-frequency AC signal passes through them. Capacitance measurement in 4070 series testers is done by applying a relatively high frequency measurement signal, selectable from 20 Hz to 1 MHz, to the DUT and then measuring the resulting current using an auto-balancing bridge circuit.

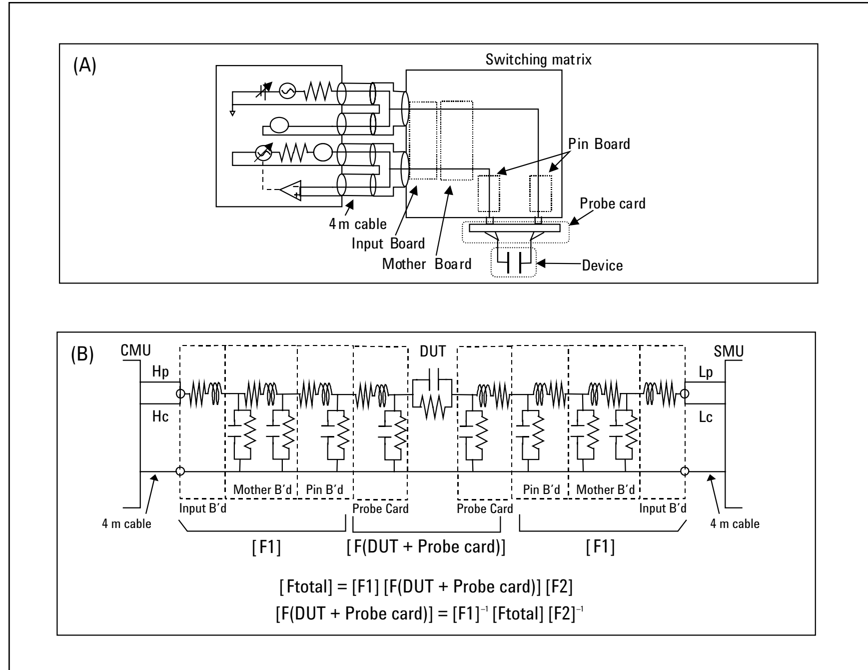

Figure 1. (A) Simplified diagram of Agilent 4070 series tester (B) Equivalent circuit of measurement path for capacitance measurement

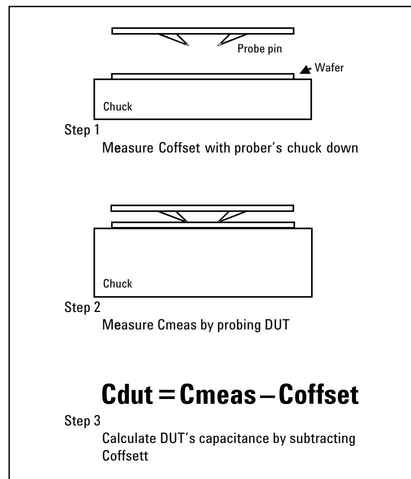

Figure 2. Procedure to cancel offset capacitance

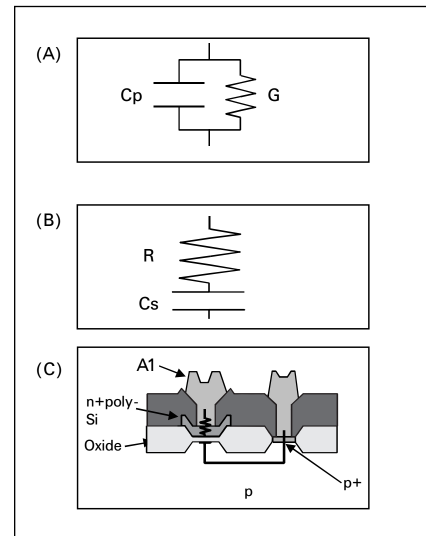

Figure 3. (A) Equivalent circuit of normal device (B) Equivalent circuit of device that has large series resistance (C) Example of device structure that has large series resistance

When measuring capacitance using a high frequency signal such as 1 MHz, stray capacitance and residual inductance inherent to cables, electrical leads, and other portions of the measurement circuit can cause AC signal loss. This leads to degradation of the capacitance measurement accuracy.

Figure 1 shows an equivalent circuit of the measurement path. The Capacitance Measurement Unit (CMU) in 4070 series testers regards the entire measurement path as the device to measure. Compensation for the cables and switching matrix is automatically performed by the Test Instruction Set (TIS) command so that the actual capacitance of the DUT is obtained. For example, the compensation for 4 m cables is performed by a built-in function of the CMU (Agilent 4284A). For a switching matrix, the actual capacitance of the DUT is calculated by multiplying the inverse matrix of the F matrix by the entire measurement value.

The circuit constants used in the F matrix are measured when the system is installed and recorded for each 4070 series tester. Therefore, precise capacitance measurement results are obtained by using TIS commands.

Offset Capacitance

The offset capacitance caused by a probe card or probe needles cannot automatically be compensated for by the TIS commands. Offset capacitance depends on the probe card used. If adjacent pins and the recommended probe card are used, the offset capacitance value would be smaller than 500 fF. To obtain the actual capacitance of the DUT, measure the offset capacitance and then measure the capacitance of the DUT. Subtract the offset capacitance from the measured capacitance. (See Figure 2.)

Series Resistance of the DUT

In most cases, semiconductor capacitors can be viewed as a parallel circuit of capacitance and conductance. Agilent 4070 series testers assume the DUT can be modeled as a parallel connection of capacitance and conductance. However, in other cases, the equivalent circuit of the device can be drawn as a series connection of resistance and capacitance. For instance, if poly-Si is used between the oxide and Al lead and the resistance of the poly-Si is relatively large compared to the impedance of the capacitance, the DUT is regarded as a series connection of capacitance and resistance. In such cases, measurement results need to be adjusted to eliminate the error caused by the incorrect assumption. The **Conv_mode** command is provided to allow you to calculate the correct capacitance value if the equivalent circuit of the DUT can be modeled as a series connection of resistance and capacitance.

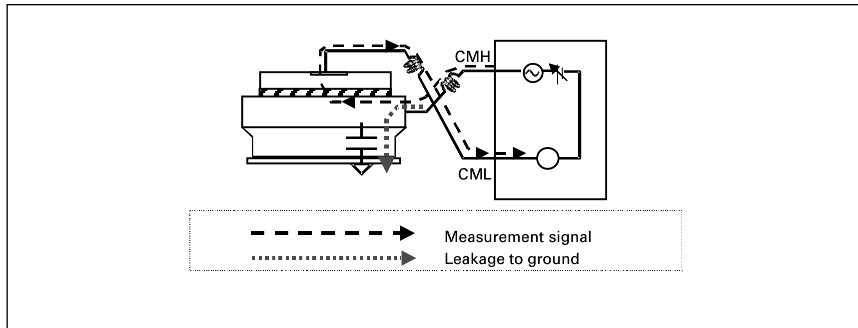

Figure 4. Unexpected leakage of measurement signal

Signal Loss Through the Large Chuck of the Prober

The capacitance between the chuck on the probe station and ground is becoming large. There are two reasons for this.

1) The size of the chuck on the probe station is increasing as wafer size increases. Capacitance is proportional to chuck size.

2) The demand for a hot chuck is increasing for process integration or process monitoring. Having the heater of the hot chuck close to the top of the chuck reduces the distance between the chuck top and ground, which results in the increase of capacitance to ground.

In many situations, the large capacitance between the chuck and ground affects the accurate capacitance measurement of the DUT.

When the chuck on a probe station is used as a measurement terminal for the capacitance measurement, the measurement current flows to ground through the chuck. Unexpected leakage of the measurement signal affects measurement accuracy. (See Figure 4.)

The same type of signal loss occurs when the isolation is insufficient between the expected measurement signal path and the chuck on the probe station.

Figure 5 shows two other typical device structures. If the electrode for the wafer substrate is placed on the top side of a wafer, an error can occur if the device structure is as shown in Figure 5(A) where the wafer substrate and probe chuck are not electrically isolated.

The device structure shown in Figure 5(B) has better isolation between the measurement signal path and the prober chuck because the PN junction formed by the N-well in the P-substrate acts as a barrier for the leakage current. The isolation level of the PN junction determines whether or not there is a signal loss to ground.

Figure 6 shows the frequency dependency of capacitance measured on the device shown in Figure 5(A). The results show that measurement error increases as the measurement frequency is increased beyond 200 kHz. The amount of error increases up to 4% at a 1 MHz measurement frequency.

When a high frequency measurement signal is used, signal loss is proportional to the residual inductance and stray capacitance along the measurement signal path. Therefore, total measurement error is proportional to the square of the measurement frequency.

In other words, if the measurement frequency is reduced by a factor of 10, then the measurement error is reduced by a factor of 100. A 4% error observed at a 1 MHz measurement frequency is reduced to a negligible level if the measurement frequency is reduced to 100 kHz.

The accuracy of a capacitance measurement is proportional to the measurement frequency. The CMU measures the current induced by the capacitance of the DUT. For an AC signal this current is proportional to the measurement frequency (I = 2 pfCV).

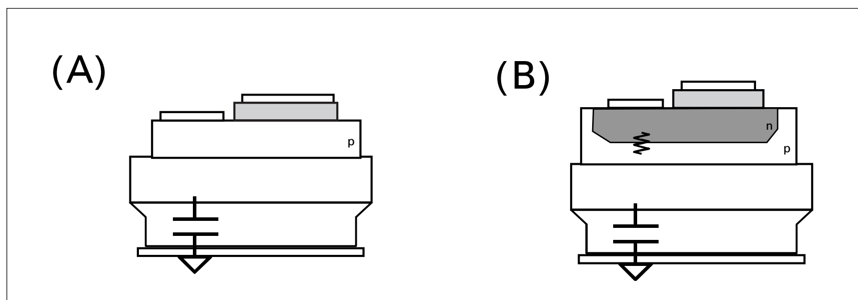

Figure 5. Device structure

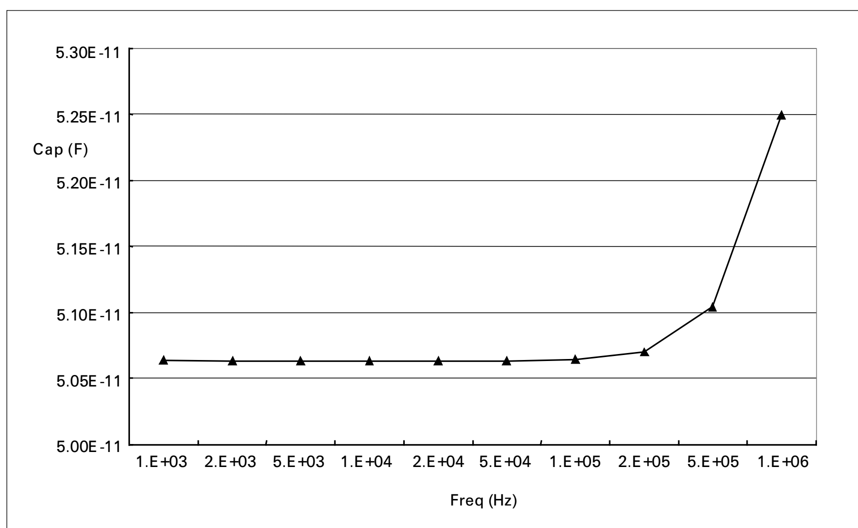

Figure 6. Frequency dependency of capacitance taken on the device structure shown in Figure 5(A)

Figure 7 shows the relationship between the standard deviation of the capacitance measured on the actual device and measurement frequency.

The results show that measurement accuracy improves as the measurement frequency is increased. It decreases when measurement frequency is over 200 kHz. This degradation at frequencies over 200 kHz is due to the effects of inductance along the signal path.

Therefore, a measurement frequency between 10 kHz and 100 kHz is recommended when measuring capacitance.

External Signal

The measurement results are affected if the measurement environment includes a large amount of electrical noise.

If the capacitance between the prober chuck and ground is large, then the chuck will likely receive high frequency noise. This is because the isolation between the prober chuck and ground is not as good in the high frequency range.

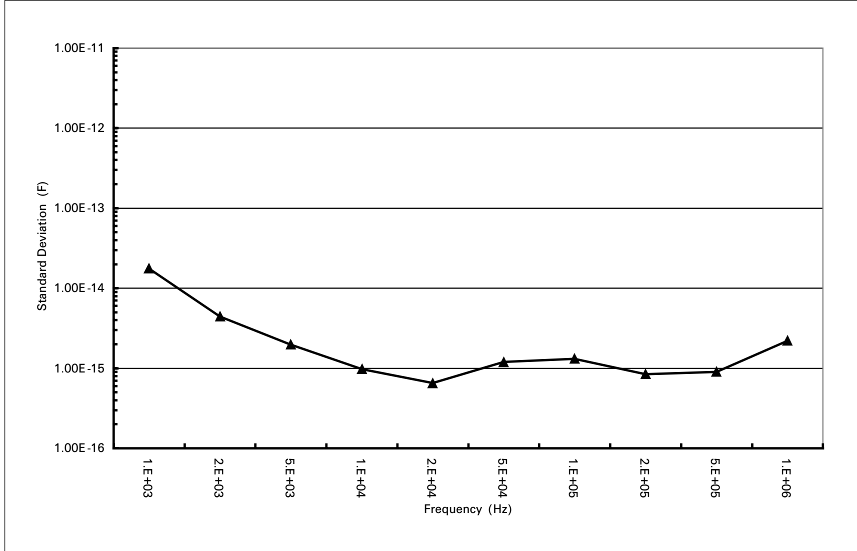

Figure 7. Frequency dependency of standard deviation of measured capacitance (Integration time: LONG)

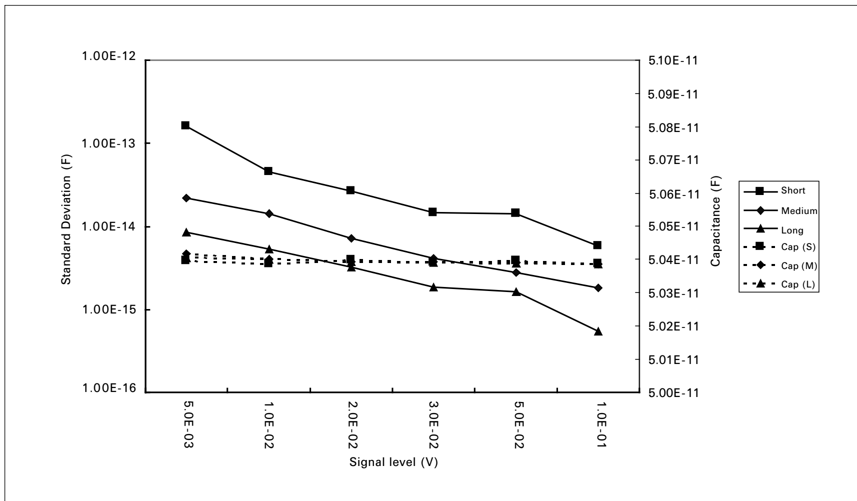

Figure 8. Signal level dependency of standard deviation of capacitance measurement

The major sources of noise in the automatic prober are the power supply circuit and the hot chuck. If sufficient shielding is provided in the prober station, then the measurement is less affected by the ambient noise.

Using a large AC signal to increase the signal-to-noise ratio will reduce the error caused by external noise.

Figure 8 shows the signal level dependency of standard deviation of capacitance measurements. Integration time is also varied from short to long. Repeatability is improved as signal level is increased. The standard deviation can be reduced to less than 1 fF by using a 100 mV signal level and a long integration time.

However, depending on the characteristics of the DUT, increasing the signal level can have a negative impact on the capacitance measurement. If C-V measurement is desired, characteristics in depletion mode can have some error because the capacitance value changes drastically with applied voltage. Signal level should be determined by considering the voltage dependency of the DUT in the swept voltage range and the required repeatability.

When evaluating oxide thickness, using a large signal level will help reduce the measurement error. Oxide thickness is calculated from the capacitance value when the DUT is in an accumulation mode that doesn't show voltage dependency.

When evaluating oxide thickness by measuring capacitance in accumulation mode, it is important to put the device well into accumulation mode. The applied bias voltage should be determined by finding the C-V characteristics where the capacitance fluctuation caused by a change in voltage is small.

Quasi-unbalanced State Caused by Improper Connection

When the capacitance between the chuck and ground is large, the connections between the measurement ports and the device terminals are important for making a precise capacitance measurement.

Figure 9 shows example measurement results taken with two different connections of the measurement ports and the device terminals. One result was measured by connecting the CMH port to the gate terminal of the device and connecting the CML port to the substrate terminal of the device. The other result was measured by connecting the CML port to the gate terminal and connecting the CMH port to the substrate terminal. When connecting the CMH to the gate terminal

a deviation of up to 7% can be seen. The opposite connection shows a stable result. This kind of error does not always occur. It depends on the DUT and the measurement environment.

The CMU in the Agilent 4070 series tester uses an auto-balancing bridge method to measure the impedance of the DUT as shown in Figure 10.

The detector D detects the potential at point A and controls the magnitude and phase of the Osc2 output so the detected potential is zero. If the measurement signal is not stable, then it becomes difficult for the auto-balancing bridge to force stabilization of the potential at point A to zero.

When the CML port is connected to the substrate terminal of a device and the substrate has insufficient isolation from the chuck on the prober, the auto-balancing bridge is likely to become unbalanced due to the large capacitance and external noise.

Figure 11 shows C-V measurement results with both connections. Clearly, connecting the CML port to the gate and the CMH port to the substrate provides better measurement results. The recommended connection is shown in Figure 12.

In this case, the polarity of the bias voltage must be taken into account when writing a measurement algorithm.

Signal Loss Through Other Devices

When the capacitance between probe pins is high and the capacitance of the adjacent device is not negligible, then an unexpected current path is formed as shown in Figure 13. In this case, additional current flows into the CML port through the stray capacitance between probe pins and the adjacent device.

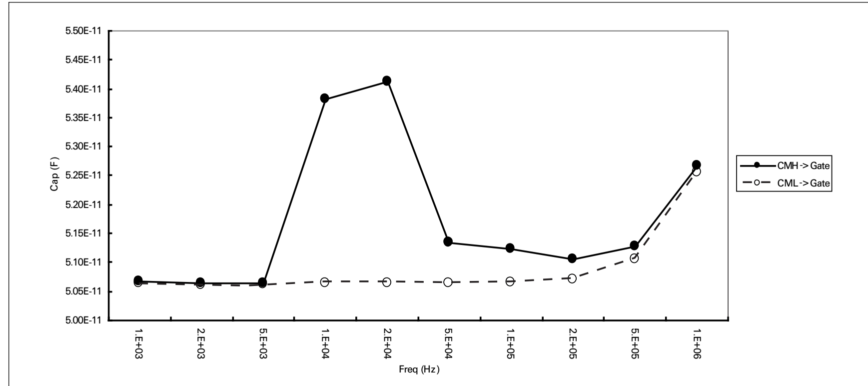

Figure 9. Measurement results with two different connections

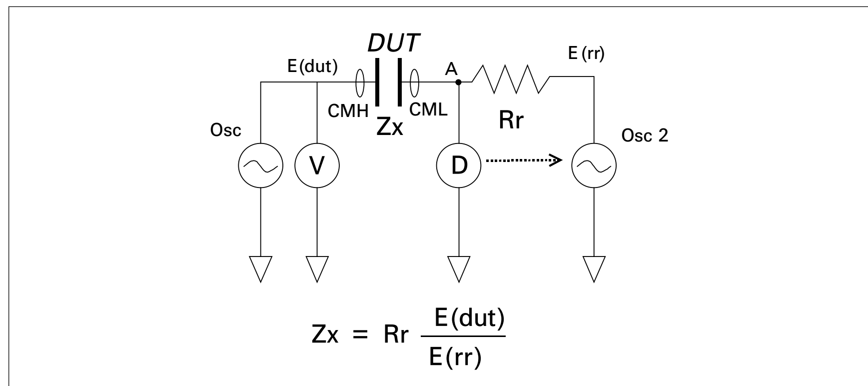

Figure 10. Auto-balancing bridge in CMU

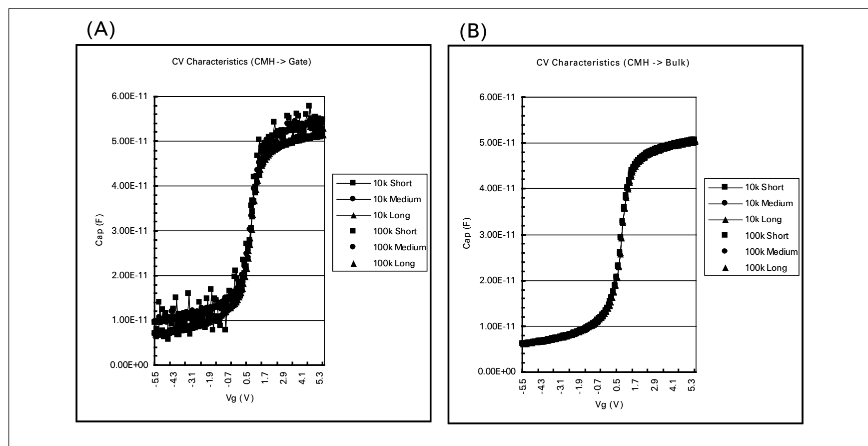

Figure 11. Measurement results with two different connections (A) Connecting CMH port to the gate terminal and CML port to the substrate (B) Connecting the CML port to the gate and the CMH port to the substrate

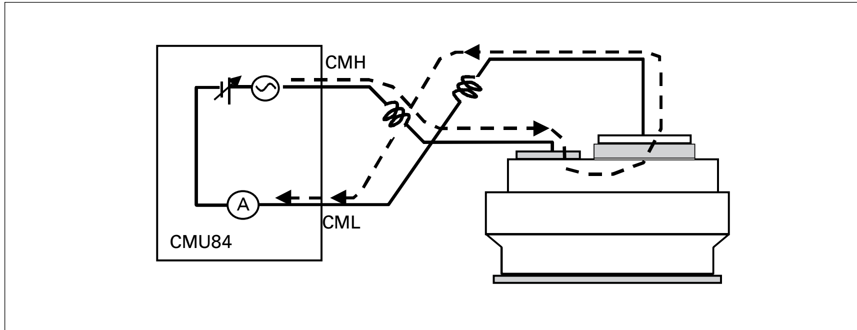

Figure 12. Recommended connection

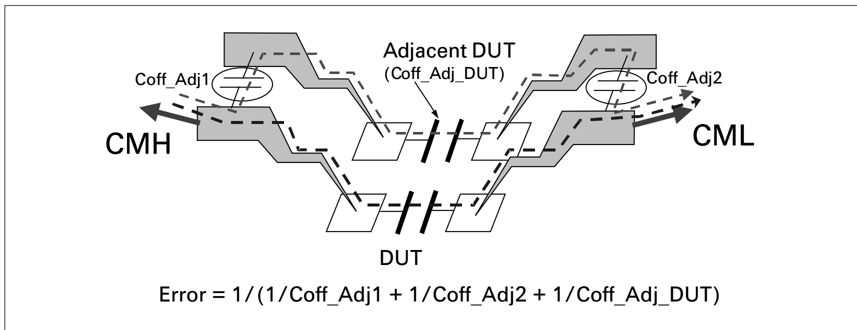

Figure 13. Unexpected current flow through other devices

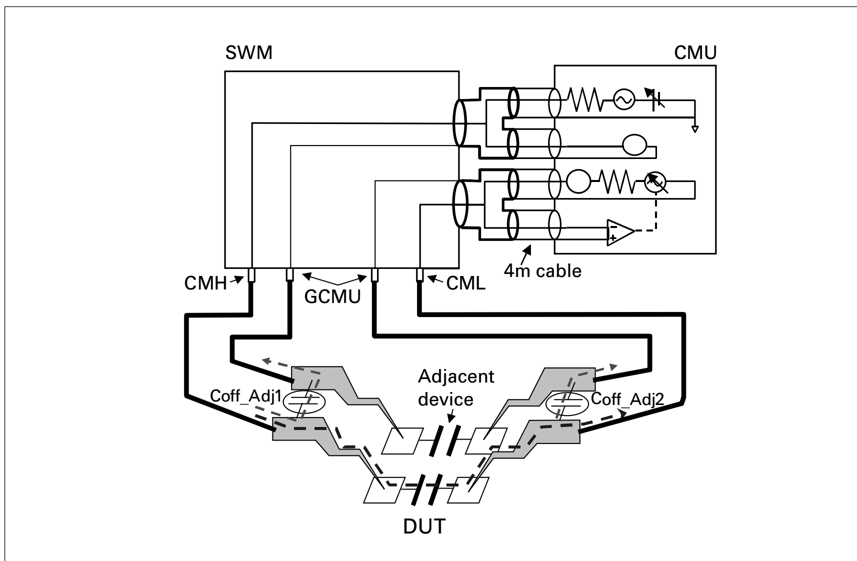

Figure 14. Reducing error by connecting the GCMU to adjacent terminals

The measured capacitance value is larger than the actual capacitance value since additional current is measured by the current meter in the CML port. The total amount of error is determined by the stray capacitance between the measurement pins and the capacitance value of the adjacent device. (See Figure 13.)

With Agilent 4070 series testers, the error caused by this mechanism will be limited to less than a couple of hundred fF if the recommended probe card is used. The problem is likely to be seen when correlating the results between the Agilent 4070 series testers and other parametric testers. Due to large stray capacitance between the probing needles, other parametric testers can exhibit an error as large as the amount of stray capacitance between the measurement pins.

There are three solutions for solving this problem.

1) Use a probe card interface and a probe card that have a small stray capacitance between the measurement pins. Reducing capacitance between pins is achieved by having a shield around the measurement pin. However, the cost of changing the probe card interface and probe card may be too great.

2) Change the test structure so adjacent devices do not have large capacitances. Stray capacitance between measurement pins is inversely proportion to the distance between the pins. Swapping the pad locations for the pins by modifying the design of the test structure will reduce this error significantly.

3) Use the GCMU to sink extraneous current flow through the stray capacitance between pins.

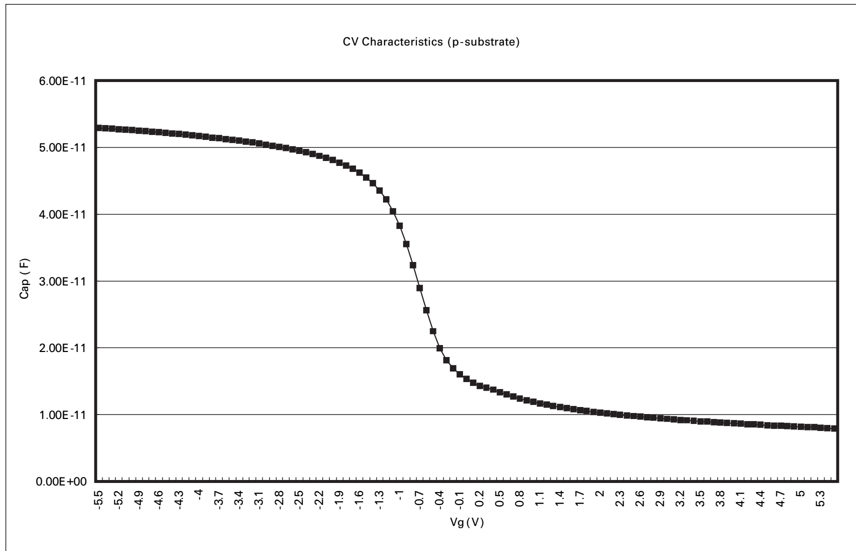

Figure 15. Example measurement results

The third suggestion is the easiest to implement. The GCMU is the shield of the CMU as shown in Figure 14. Extraneous current, going through stray capacitance between pins, will flow into the GCMU. This is because the impedance of the GCMU is lower than the impedance of the adjacent device. Additional current will not be measured by the current meter in the CML port. For example, this method will not work when the impedance between the measuring pad and the adjacent pad is low. However, it should be the first method tried when the capacitance measured by the other tester is larger than that measured by the 4070 series tester.

Conclusion

Agilent 4070 series testers can perform accurate and repeatable capacitance measurements. (See Figure 15.) The following conditions are necessary for the system to reach its full potential:

1) The offset capacitance must be subtracted in the user's measurement program.

2) When the series resistance in the DUT is large, compensation by using the Conv_mode command is required.

3) A measurement frequency between 10 kHz and 100 kHz should be used in order to avoid signal loss caused by the large capacitance of the chuck.

4) A higher signal level is recommended to reduce the effect of external noise.

5) To reduce noise and to reduce unbalance of the CMU, it is important to connect the CMH port to the bulk or substrate and to connect the CML port to the gate.

6) An appropriate probe card that has small stray capacitance between pins is required.

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